

10/814, 943

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 001207.P011	Application Number: Not yet assigned
		First Named Inventor: Peter M. Pani	
		Filing Date: Herewith	

## U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code <sup>2</sup>	Kind (If known)			
Wan		4,912,342		Wong, et al.	3/1990	
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		Office <sup>3</sup>	Number <sup>4</sup>	Kind (If known)				

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1		5,256,918		Suzuki	10/1993	
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W/		5,396,126		Britton, et al.	3/7/95	
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WTW		5,550,782		Cliff, et al.	8/27/96	
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<i>OT</i>		EPO	0415542		Advanced Micro Devices, Inc.	3/6/91		
		EPO	0630115A2		Pilkington Micro-Electronics Limited	6/1/94		
		PCT	9410754		Xilinx, Inc.	5/11/94		
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**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
VM		Altera Corporation Date Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
VM		ATMEL Field Programmable Arrays, AT6000 Series, 1993, p. 1-16. Co-processor Field Programmable Gate arrays AT6000(LV) Series, 10/99, Page 1-27.	
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VM		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5. 1/88	
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#### OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
UTan		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 2 pages.	
UTan		Robert H. Krambeck, "ORCA: A High Performance, Easy to Use SRAM Based Architecture", p. 310-320, Wescon September 28-30, 1993.	
UTan		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
UTan		Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting, "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages, Actel Corporation. <u>No date</u> .	
UTan		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
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UTan		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
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		Xilinx, "The Programmable Gate Array Data Book", 1992. <u>only table of contents Scanned</u> . <u>UTan</u>	

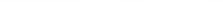
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